The Anti-Circuit Concept For the Characterization of Active Circuits Using Electromagnetic Simulations

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Abstract— **The anti-circuit is introduced as a new concept in network theory. A new technique based thereupon, for the combination of electromagnetic field simulations of planar circuits and the analysis of complex active circuits is proposed. This technique allows the incorporation of passive lumped elements as well as the passive metallization of active components into electromagnetic simulations and provides a simple interface for active and nonlinear simulations.**

I. Introduction

In order to reduce the development cost and to shorten the development cycle of electromagnetic high frequency (HF) circuits, developers use computer-aided design (CAD) techniques to predict the performances of the circuit even before it is ever built. For lower frequencies and simple structures, algebraic and heuristic formulas suffice. As frequencies and complexity increase, more performing simulators must be used. Nowadays circuit simulators are quite popular and have become a standard tool for a developer. For dense and complex structures with strong or important parasitic couplings, the accuracy of these circuit simulators is often limited. In those cases electromagnetic simulators are of growing importance.

Electromagnetic field (EM) simulations based on the method of moments (MOM) are highly accurate and applicable to high frequency planar circuit design [1]–[4]. Most commercially available EM solvers can only handle passive planar structures. However, HF design requires the integration of active devices, e.g. transistors and diodes, and lumped elements, e.g., decoupling capacitors, into the circuits.

The compression approach (CA) of Kunisch and Wolff [5] allows the combination of passive linear parts (that can be solved by an EM solver) with nonlinear or active parts in hybrid circuits. This technique was combined with the MOM in [6]. In this way lumped elements are directly included in the electromagnetic simulation (reducing the overall circuit simulation time) while inner ports provide an interface for plugging in active or nonlinear devices in a nonlinear simulation.

The technique proposed in this paper allows the characterization of the passive metallization part of active circuits, by using internal parallel ports and a new de-embedding scheme. This technique is based on the CA [5] and [6], extending it with principles from circuit theory.

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In recent technological developments, e.g., in active antennas [7]–[11], the active component is included into the radiating circuit. Though the active device itself may be well characterized, the influence of the increased coupling with the passive part makes reliable design difficult [9] and [11] and asks for the characterization of the field coupling of active devices with the rest of the circuit. The CA [5] allows for the characterization of all passive parts in one simulation. The inclusion of the passive metallization of active devices however, is quite cumbersome. The new technique described in this paper takes into account the coupling between all passive parts, including the metallization of the active element, during the electromagnetic simulation, and thus characterizes the field coupling in the complete circuit. Some post-processing based on the anti-circuit concept allows for the use of standard CAD device models for the nonlinear simulation.

The technique can also be adapted for the de-embedding of the planar connection paths during measurements of active devices, where calibration standards are not available.

In a recent publication [12], Bosy *et al.* included the wave characteristics of the device metallization and the input circuits of a distributed FET in order to improve the characterization of the FET. Their approach uses approximative and heuristic formulas to account for those characteristics in a very simple case. Our approach is more general and includes all passive metallizations in an exact way.

This paper, which elaborates on the ideas stated in [13], is organized as follows. In Section II the CA of Kunisch and Wolff is outlined together with some shortcomings. Section III introduces the concept of the anti-circuit which is used in Section IV to derive the new simulation strategy. Section V illustrates our technique via a case study, followed by some conclusions in Section VI. Finally Appendix A explains the mixed potential integral equation (MPIE) formulation of Maxwell's laws and Appendix B explains the equivalent circuit interpretation when applying the MOM to the MPIE. Dimensions for the FET structures in the case study can be found in Appendix C.

II. Compression Approach

The characteristics of a linear circuit are independent of the amplitude of the excitation and can be simulated relatively easily and quite accurately [1], [2], [4], [6]. The characteristics of nonlinear circuits are (highly) dependent on the excitation and the simulation becomes time consuming.

A way to circumvent this problem is to segment the hybrid circuit into several linear and nonlinear segments. This is

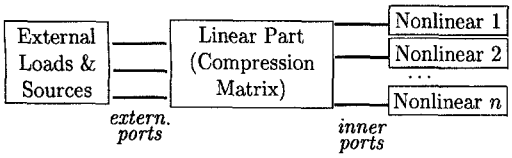

Fig. 1. Schematic of the CA.

the typical circuit simulator approach. Each segment is simulated using an appropriate technique and is connected to its neighbors using circuit and system theory. This segmentation technique does not take the coupling between the different segments (apart from port currents and voltages) into account. With increasing frequencies and for denser structures, this (field) coupling becomes stronger and hence more important.

Kunisch and Wolff solved this problem by their CA [5], which takes the coupling between all passive parts into account. As can be seen in Fig. 1, the hybrid circuit is considered to be the superposition of a single linear part governed by Maxwell's laws, and a number of small isolated nonlinear groups consisting of nonlinear and/or active elements [5], for which Kirchhoff's laws hold. This is feasible because the dimension of each separate group is small, and because the nonlinear groups are not directly interconnected; port voltages and currents can be defined meaningfully and are used for connection with the single linear part via inner ports. Interconnections between the nonlinear groups are forbidden as currents and voltages have no clear definition nor meaning in defining a relationship between those groups.

The block of external loads and sources—needed for the nonlinear characterization—is connected to the linear part by external ports under the assumption of fundamental mode propagation [5], [6].

The nonlinear characterization is divided into two steps. In a first step, the passive linear part is simulated e.g. with a MOM technique or with the finite difference time domain (FDTD) technique as in [5], and the matrix of the resulting S-parameters form the compression matrix. In the second step the compression matrix is combined with the external loads and sources and the different nonlinear groups into a nonlinear simulation. If loads or sources change, only the nonlinear simulation has to be repeated, and not the complete characterization.

Remark that there is no field coupling between the nonlinear groups and the linear part, only coupling via the inner ports is allowed. For higher frequencies, the performance of the linear space domain metallization might be influenced by the presence of the large passive metallization of a nonlinear element, such as a FET. The CA states that this passive metallization should be included into the single linear part. But then it becomes quite cumbersome to define the inner ports in an appropriate way. And even then, the characterization of the nonlinear region is quite difficult. On the other hand, most available nonlinear devices have already been accurately characterized and modeled with their metallization included. The development of a technique which allows to take advantage of existing device models (including their metallization) but at the same time accounts for the coupling between the device metallizations and the other parts of the passive planar circuit is the aim of this paper.

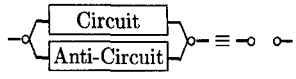

Fig. 2. Definition of anti-circuit.

III. Anti-Circuit Concept

Our new technique is based upon a new concept in circuit theory: the anti-circuit. Its definition is purely mathematical, it has no physical meaning. The anti-circuit is defined as the circuit which, placed in parallel with the the original circuit, results in an open circuit (Fig. 2). As a circuit is most often characterized by its scattering parameters (S-parameters), the S-parameter representation of the anti-circuit is derived next.

Theorem: $S_{anti} = S^{-1}$

Proof: Circuit theory states that if circuits 1 and 2 are connected in parallel, the total circuit t can be described by $Y_t = Y_1 + Y_2$. The S-matrix and the Y-matrix (admittance matrix) description are related through $S = (1+Y')(1-Y')^{-1}$ and $Y' = (1+S)(1-S)^{-1}$ in which Y' represents the normalized Y-matrix, i.e. the admittances are normalized to the reference impedances (R_i for port i) of the scattering parameters: $Y'_{ij} = \sqrt{R_i R_j} \cdot Y_{ij}$. The open circuit Y-matrix is the null matrix, so $Y_{anti} = -Y$ and also $Y'_{anti} = -Y'$. Hence

$$\begin{aligned} S_{anti} &= (1 + Y'_a nti)(1 - Y'_{anti})^{-1} \\ &= (1 + (-Y'))(1 - (-Y'))^{-1} \\ &= (1 - Y')(1 + Y')^{-1} \\ &= ((1 + Y')(1 - Y')^{-1})^{-1} \\ &= S^{-1} \end{aligned}$$

■

The anti-circuit will be one of the key elements in our new technique.

IV. Simulation Strategy

First, some terms are introduced, using a FET as an example (Fig. 3). A hybrid circuit "Circuit" [the active FET and its matching networks, Fig. 3(a)] consists of a (distributed) passive network "*Pass.Netw.*"—including both the ordinary metallization and the lumped elements [6]—[the matching networks with decoupling capacitors in our example, Fig. 3(b)] and an active device "*Device*" [in this case the FET itself, Fig. 3(c)]. The passive metallization of the device itself is referred to as the device metallization "*Dev.Metal.*" [the FET fingers forming an interdigital capacitor, Fig. 3(d)]. This is the metallization we want to include in our simulation.

The passive network "*Pass.Netw.*" and the passive metallization "*Dev.Metal.*" are grouped into the linear part "*Linear*," as required by the CA [5], [6]. Parallel ports are introduced at the interface between the passive network and the device metallization. The total linear part is simulated with an electromagnetic simulator (based on a MPIE formulation of Maxwell's laws and a MoM approach [1], [2]; we refer

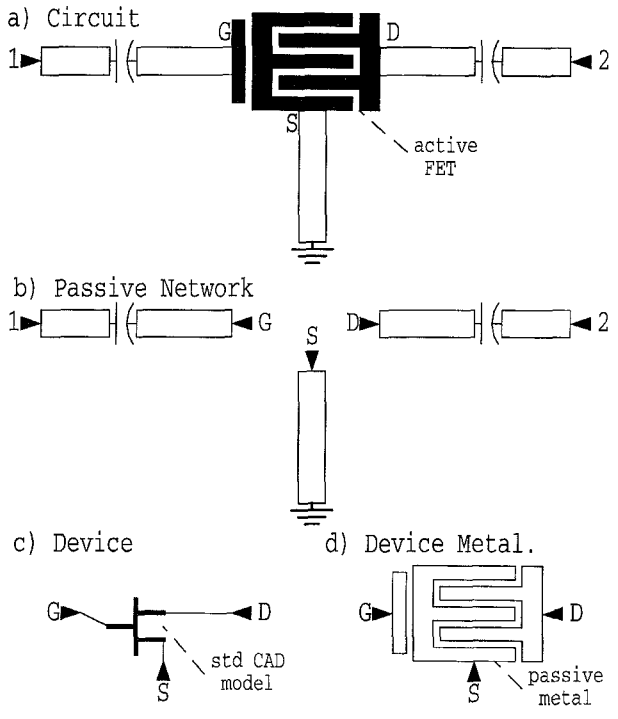

Fig. 3. A FET as illustration of our technique.

to the Appendix for some more details). The resulting S-parameters S_{Lin} characterize (1) the passive network as well as (2) the device metallization and (3) the coupling between both. A standard CA would only find part (1). The device metallization characterization (2) is normally already included in the CAD model for the device. (3) however is the extra coupling included by our new technique and must be preserved in the final S-parameters, together with the passive network characteristics. The characteristics of the device metallization (2) are now eliminated using the anti-circuit principle introduced above.

How this de-embedding is achieved, is explained below (Fig. 4).

1) The "*Circuit*" consists of the "*Passive Network*" in series with the "*Device*" (standard compression approach [5], [6]). Symbolically the "*Device*" can be written as the "*Device Metallization*" in parallel with the "*Device Nonlinearities.*"
2) The "*Passive Network*" and the "*Device Metallization*" are combined into the "*Linear*" part.
3) Next an "*Open Circuit*" is added in parallel to the "*Device Nonlinearities,*" this doesn't change its characteristics. By definition it can be substituted by the "*Device Metallization*" in parallel with its "*anti-circuit.*"
4) The "*Device Metallization*" is again combined with the "*Device Nonlinearities*" into the "*Device.*"
5) This yields that the "*Circuit*" can be written as the "*Linear*" part in series with the "*Device*" parallel to the "*Anti-Device-Metallization.*"

Summarizing, two electromagnetic simulations have to be performed: one for the complete linear part (S_{Lin}) and one for the device metallization (S_{DM}). The S-parameters of the anti-

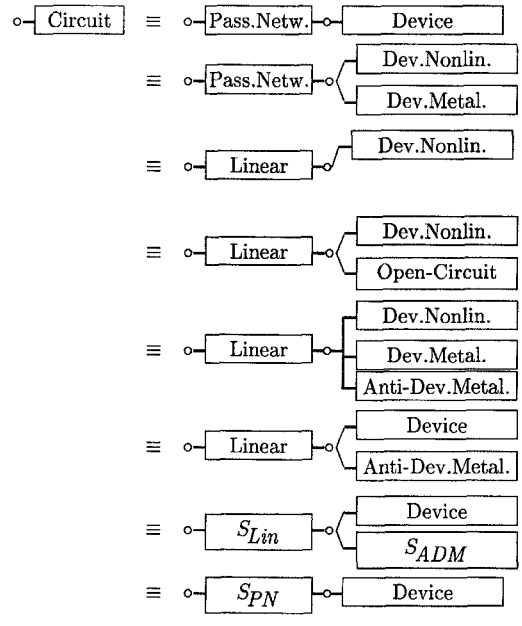

Fig. 4. De-embedding of the device metallization from the linear simulation.

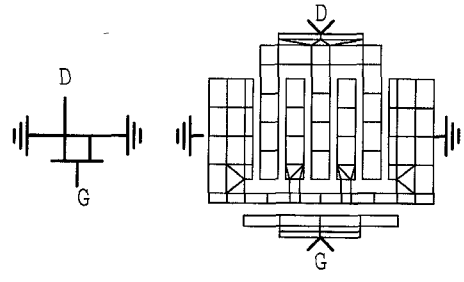

Fig. 5. Layout of a single FET.

device-metallization are then given by $S_{ADM} = (S_{DM})^{-1}$. The sought-for S-parameters S_{PN} of the passive network, including the coupling with the device metallization, are found through

$$\begin{aligned} S_{PN} &= (1 + Y'_{PN})(1 - Y'_{PN})^{-1} \\ &= (1 + (Y'_{Lin} + Y'_{ADM}))(1 - (Y'_{Lin} + Y'_{ADM}))^{-1} \end{aligned}$$

or finally

$$S_{PN} = (1 + Y'_{Lim} - Y'_{DM})(1 - Y'_{Lin} + Y'_{D})^{-1} \quad (1)$$

with

$$\begin{aligned} Y'_{Lin} &= (1 + S_{Lin})(1 - S_{Lin})^{-1} \\ Y'_{DM} &= (1 + S_{DM})(1 - S_{DM})^{-1}. \end{aligned} \quad (2)$$

V. Case Study: Three Coupled FET's

A. Description and Layout

The use of our technique is illustrated through the characterization of three coupled field effect transistors (FET's). Each FET has a gate width of six times 100 μm and is grown on a 450 μm thick GaAs substrate ($\epsilon_r = 12.9$). The sources of the FET's are grounded.

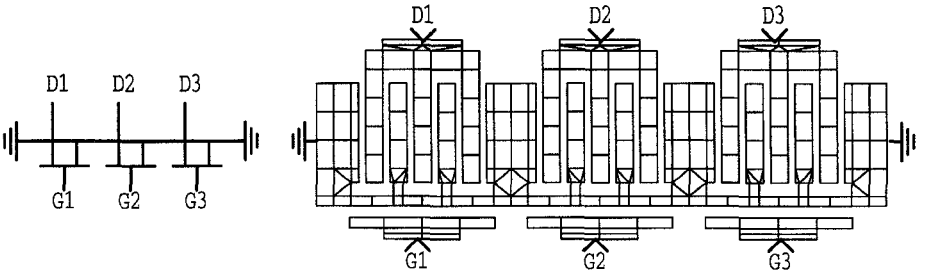

Fig. 6. Layout of a triple FET.

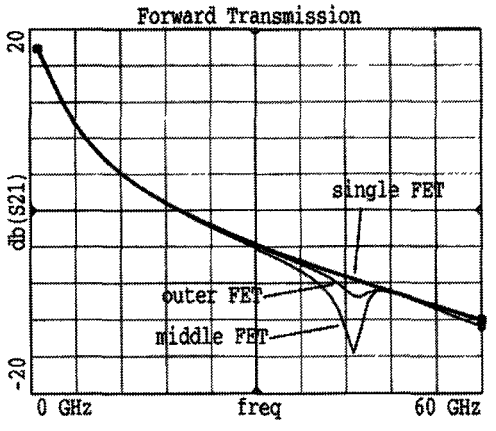

Fig. 7. S-parameters for the forward transmission (S_{21}).

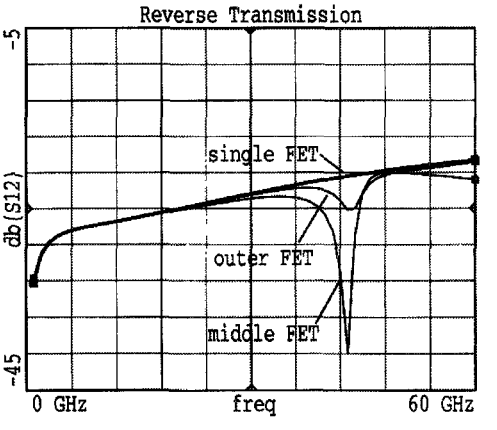

Fig. 8. S-parameters for the reverse transmission (S_{12}).

First, a single FET (symbolically shown at the left of Fig. 5) was grown and characterized by a ROOT model, extracted from measurements [14]. Next its device metallization, including the drain and source fingers as well as the gate and drain ports, was simulated using the mesh shown at the right of Fig. 5. The S-parameters resulting from the electromagnetic simulation were inversed yielding the S-parameters of the anti-circuit of the device metallization. The metallization of the gate electrodes is not taken into account in the electromagnetic simulations. As their surface is much much smaller than those of the source and drain fingers, their (passive) electromagnetic coupling with the other passive metallizations will be much smaller and thus negligible.

Next we characterized the triple FET (symbolically shown at the left of Fig. 6) by our technique described above. We calculated the S-parameters of its device metallization by an electromagnetic simulation (the mesh is shown at the right of Fig. 6). We added the linear anti-device-metallization of the single FET and the nonlinear ROOT model of the single FET, in parallel over each of the three gate-drain couples to the device-metallization of the triple FET. Thus we obtained our model for the three coupled FET's. Finally, we performed some S-parameter and harmonic balance analyzes on this model using the HP-MDS simulator [15]. Some of the results are presented below.

B. S-Parameters

The S-parameters of the three coupled FET's were simulated by applying S-parameter ports with 50 Ω reference impedances to each of the six ports ($G1, D1, G2, D2, G3, D3$) of our model. The frequency was swept from 1 GHz up to 60 GHz. As the normal signal propagation in a FET is from the gate to the drain, this propagation direction is labeled as the forward transmission or S_{21} characteristic. The propagation from the drain to the gate is labeled as the reverse transmission or S_{12} characteristic. A good FET has a high forward and a very low reverse transmission.

Fig. 7 shows the forward transmission characteristics (S_{21}) for the different FET's, whereas Fig. 8 shows the corresponding reverse transmission characteristics (S_{12}). In these figures only corresponding gates and drains are considered. Three sets of curves are shown: one for the single FET of Fig. 5; one for FET 1 and FET 3 of Fig. 6, i.e., the outer FET's which are equal because of symmetry; and one for FET 2 of Fig. 6, the middle FET.

The forward transmission curves for the triple FET coincide with the one for the single FET except for a dip around 45 GHz. This phenomenon, which is of more influence to the middle FET, is probably due to the excitation of a substrate mode. The same applies to the reverse transmission curves.

The S-parameter analysis of the triple FET also yields the cross-coupling between the three coupled FET's, i.e., the influence of an excitation at the gate of FET 1 on the drain of FET 2 or FET 3 (cross-coupled forward (S_{21}) transmission) or of an excitation at the drain of FET 2 on the gate of FET 1 (cross-coupled reverse (S_{12}) transmission). Now these non-corresponding gate-drain pair characteristics are considered. Again, three sets of curves are displayed: one for the direct transmission, i.e. the single FET characteristics—also shown in Fig. 7 and Fig. 8; one for the transmission from FET 1 to FET

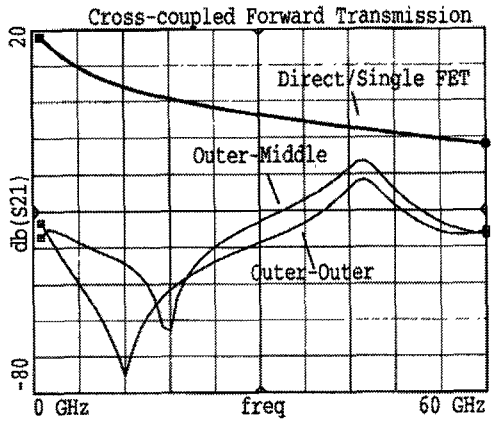

Fig. 9. S-parameters for the cross-coupled forward transmission (S_{21}).

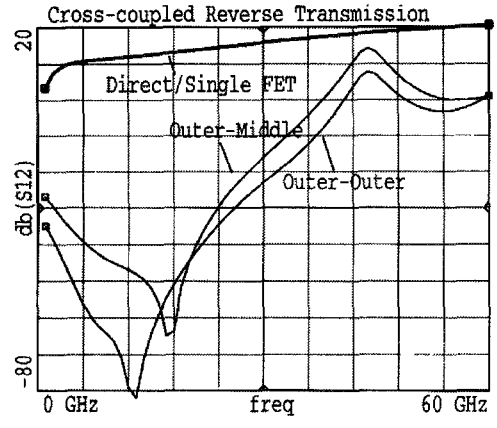

Fig. 10. S-parameters for the cross-coupled reverse transmission (S_{12}).

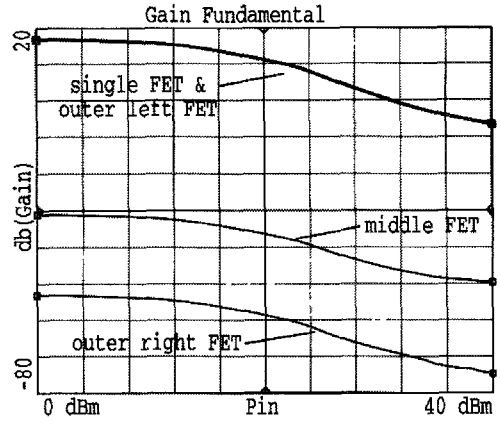

Fig. 11. Fundamental gains, as a function of the input power (excitation at the gate of the outer left FET at 10 GHz).

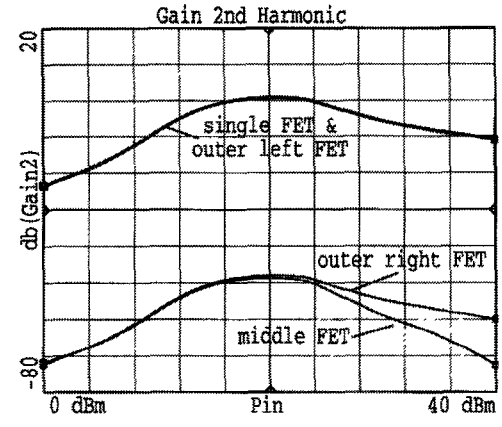

Fig. 12. Gains for the second harmonic, as a function of the input power (excitation at the gate of the outer left FET at 10 GHz).

2, the Outer-Middle transmission; and one for the transmission from FET 1 to FET 3, the Outer-Outer transmission. The characteristics from FET 2 to FET 1 (Middle-Outer) almost coincide with those from FET 1 to FET 2 (Outer-Middle) and are therefore not shown here. Due to symmetry, FET 1 and FET 3 may be interchanged.

The curves in Fig. 9 and Fig. 10 reveal that our technique is able to predict coupling between active elements due to the coupling between the passive metallizations of the different FET's. The cross-coupling characteristics remain always more than 20 dB below those for the single FET, except for the frequency range from 40 GHz to 55 GHz. This region, which corresponds with the dip regions in the curves on Fig. 7 and Fig. 8, shows that stronger coupling occurs, probably via the excited substrate mode. Again the middle FET seems to be more sensitive to coupling than the outer FET's.

C. Harmonic Balance

The prediction of the nonlinear characteristics was performed via a harmonic balance analysis. The input power at one of the gates was swept from 0 dBm to 40 dBm for a constant frequency of 10 GHz. All ports were loaded with 50 Ω impedances. The output amplitudes at the different ports of the different harmonics were related to the amplitude of the fundamental frequency at the input port in order to calculate the gains.

In a first simulation the gate of the outer left FET was excited. Figs. 11 and 12, respectively, show the gain of the fundamental frequency and the gain of the second harmonic at the different output ports (the drains). The throughput for the single FET and for the triple FET coincide for both figures. As a result of applying our technique the cross-coupling can be clearly detected. The fundamental mode (Fig. 11) at the middle FET (caused by the excitation at the outer left FET) is approximately 20 dBm stronger than the fundamental mode at the outer right FET, and 45 dBm weaker than the direct throughput. This can also be seen in the characteristics for the linear S-parameters in Fig. 9 at the frequency of 10 GHz. For the second harmonic (Fig. 12) both amplitudes are equal for lower input powers, and approximately 50 dBm weaker than the direct throughput. Again this can seen in Fig. 9 at the frequency of 20 GHz. From about 20 dBm input power the nonlinearities for the middle FET start to differ from those from the outer FET: the second harmonic at the middle FET gets (almost linearly) weaker than that of the outer right FET. The difference between the latter and the direct throughput remains at -50 dBm.

A similar harmonic balance analysis was also performed for excitation at the gate of the middle FET, FET 2, yielding similar results.

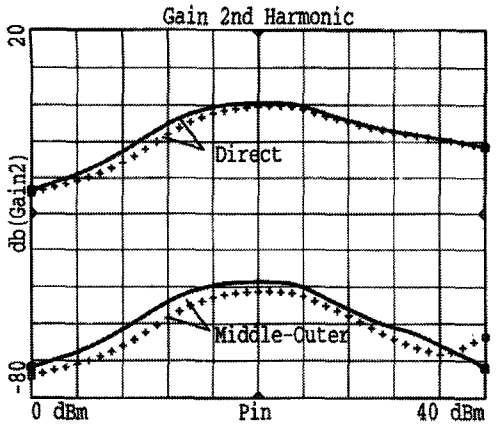

Fig. 13. Magnitude of fundamental gain, calculated with (solid line) and without (crosses) anti-circuit, as a function of the input power (excitation at the gate of the middle FET at 10 GHz).

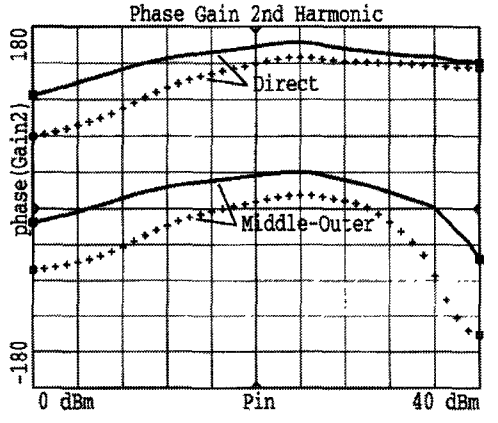

Fig. 14. Phase of fundamental gain, calculated with (solid line) and without (crosses) anti-circuit, as a function of the input power (excitation at the gate of the middle FET at 10 GHz).

In order to show the influence of the anti-circuit, the same harmonic balance analysis was performed on a model for the triple FET without putting the anti-device-metallization of the single FET in parallel over each gate-drain pair. A comparison between both sets of curves (with and without the use of the anti-circuit) is given in Figs. 13 and 14 for, respectively, the magnitude and the phase of the gain of the second harmonic at the different output ports. There are only two transmission curves: one for the direct throughput (from the middle gate to the middle drain, which coincides again with the curves for a single FET) and one for the Middle-Outer characteristic (from the middle gate to an outer drain). The thick lines indicate the results with anti-circuit, the crosses those without.

The amplitude of the gains (Fig. 13) doesn't differ that much, but the difference in phase (Fig. 14) is much larger, about 36 degrees for the Middle-Outer characteristic. The differences between the gains of the fundamental frequency are less, but those of the third harmonic are even larger—, up to 6 dB for the amplitude and 50 degrees for the phase (both sets of curves are not shown here). This can be explained by the fact that the passive metallization of the single FET acts as an interdigital capacitor. Omitting the parallel anti-device-metallization is the same as putting that interdigital capacitor in parallel. For lower frequencies, a capacitor in parallel does not change the characteristics considerably. As the frequency increases, the coupling between the fingers increases and the influence of the capacitor becomes stronger and more apparent.

VI. Conclusion

In this paper we introduced the new anti-circuit concept. We also proposed a new simulation strategy, extending the compression approach. These improvements allow for the inclusion of the (passive) metallization of active components into electromagnetic simulations, and thus for a better characterization of active circuits. In this technique standard CAD device models are used. The technique is illustrated by an S-parameter and a harmonic balance analysis of three coupled FET's.

Appendix

A. Maxwell's Laws and the Method of Moments

In our approach, the electromagnetic simulation for planar circuits, is based on the mixed potential integral equation (MPIE) formulation of Maxwell's laws [1], [2]

$$\int_S dS'(G_a(\vec{r};\vec{r}')\vec{J}(\vec{r}') - \vec{\Delta}_t(G_e(\vec{r};\vec{r}')\vec{\Delta}_t \cdot \vec{J}(\vec{r}'))) + Z_S(\vec{r})\vec{J}(\vec{r}) = -\vec{E}_t(\vec{r}) \tag{3}$$

with S the metallization surface and Z_S the surface impedance of the metallization, $\vec{E}_t^{\,\text{in}}$ the tangential incident electric field, $\vec{J}$ the current distribution and G_a the magnetic and G_e the electric Green's function for the layered medium. The MOM [2] and [16] transforms this MPIE into the matrix equation

$$\sum_{n=1}^{M} Z_{m,n} \cdot I_n = V_m, \qquad m = 1 \cdots M \tag{4}$$

e.g., using rooftop functions both for expansion and for weighting functions. Z is the cell-cell interaction matrix, I the coefficient vector of the rooftop expansion functions and V the excitation vector.

B. Equivalent Circuit Interpretation

The interaction matrix Z can be interpreted in terms of a circuit equivalent of the meshed circuit (Fig. 15): the cells in the mesh represent the nodes of the network. Each node has a capacitor to the ground; the mesh sides and their discretized surface currents are translated into inductive branches. All capacitors and inductors are mutually coupled. The interaction matrix equations merely express Kirchhoff's voltage laws applied to the equivalent circuit.

C. Dimensions in the Case Study

The gate feedlines are 80 μm wide; the gate port is 154 μm wide and 11 μm long.

The source metallization between the gate (separation of 12 μm) and the FET fingers (separation of 14 μm) is 223 μm wide and 10 μm long. The connections with the source fingers

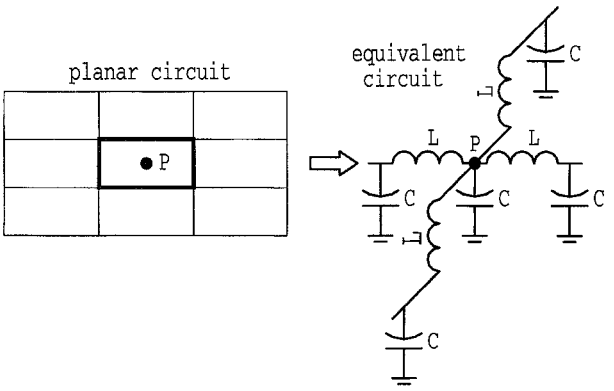

Fig. 15. Equivalent circuit interpretation of the interaction matrix.

are 10 μm wide (and 14 μm long). Both the source and the drain FET fingers are 18 μm wide, 100 μm long and 7.5 μm seperated from each other. The outer source metallization is 36 μm wide and 124 μm long $(10+14+100)$; the half fingers connected to it are 8 μm wide.

The drain feedlines are 84 μm wide; the drain port is 120 μm wide, 19 μm long and 12 μm seperated from the FET fingers. The connections with the drain finger are as wide as the fingers themselves, i.e., 18 μm.

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